Monolithic Dual-Gate GaAs FET Digital Phase Shifter

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Abstract—**The design, fabrication, and characterization of a fully monolithic FET digital phase-shifter circuit is described. The circuit is designed around a unique dual-gate FET structure operating as a switchable single-pole, double-throw amplifier. Each 2.5×3.0-mm chip has one bit (e.g., 22.5°, 90°, etc.) of phase control. The circuit, which includes all dc bypass circuitry on-chip, features thin-film lumped element capacitors and inductors, air-bridge crossovers and interconnects, via-hole frontside grounding, and integral beam leads. The fabrication of these elements is described in some detail. The phase-shifter circuit gives a peak gain of 3 dB across a 10-percent bandwidth in *X*-band. A method of achieving continuous phase and amplitude control using a 90° bit chip is described. Finally, phase performance of a four-bit digital phase shifter realized by cascading four monolithic active phase-shifter chips is reported.**

I. INTRODUCTION

MONOLITHIC microwave integrated circuits (MMIC's) fabricated on GaAs offer the potential for significant reductions in size, weight, and cost, along with increased reliability over conventional hybrid microwave components. These advantages are particularly attractive in applications involving electronically agile active phased-array antennas. Such antennas consist of an ensemble of closely packed (on the order of a wavelength) radiating elements each of which is driven by a microwave transmit/receive (T/R) module circuit. By controlling the phase of the output of each element in the array, the composite beam is steered and shaped electronically.

A key element in the phased-array T/R module circuit is obviously the phase shifter itself. This phase shifter can be passive, such as is the case for the conventional high-pass, low-pass p-i-n diode type [1], [2], or it can be active, providing phase shift with gain rather than insertion loss. Recently, a number of active phase-shifter circuits have been designed in various laboratories using GaAs field-effect transistors (FET's) and, in particular, dual-gate FET's (DGFET's).

Two fundamentally different approaches have been used to realize active phase-shifting circuits using DGFET's. The first of these makes use of the variation of the phase of S_{21} of the circuit with changing bias conditions on one or both of the device's gates. Using this approach, a single-device circuit demonstrating 120° of linear continuous phase control and 4 dB of gain at 12 GHz has been obtained [3]. A three-device subassembly with 140° of phase variation and up to 30 dB of gain was also reported at 12 GHz [4]. Other workers [5] have studied phase shifting versus gain characteristics of DGFET's as a function of both gate voltages and discussed the design of *S*-band phase-shifting circuits using such devices. These types of phase shifters are inherently narrow band and have a phase sensitivity that is strongly dependent on the FET characteristics.

The other approach which has been taken to achieving active phase shifters has been to use dual-gate FET's as switchable amplifiers which allow different phase length paths to be chosen, singly or in combination, to achieve the desired phase shift. This technique has been used to produce a broadband (4–8 GHz) continuous 360° phase shifter with minimal loss over the band [6], [7]. A *Ku*-band (16 GHz) continuous 360° phase-shifter circuit has also been reported with gain control from −6 to −28 dB [8]. These circuits, like the ones discussed above, are both hybrid and thus not suited to those applications where MMIC's are required.

In this paper, we will present the first demonstration of a monolithic active phase-shifter circuit. The circuit is designed around a unique dual-gate FET switchable amplifier. It provides about 3-dB gain over a 10-percent bandwidth in *X*-band. The circuit is designed to provide a discrete unit of phase shift relative to some reference phase delay. We will show how the individual circuits are cascaded to form a four-bit digital 360° phase shifter with gain. Additionally, we will describe how the circuit can be used to provide continuous phase control over 360° with automatic amplitude tapering—both desirable characteristics for phased-array elements.

II. PRINCIPLE OF PHASE SHIFTER

The concept on which the active phase-shifter design is based is presented schematically in Fig. 1. This diagram shows two DGFET's in a single-pole, double-throw (SPDT) configuration. It is assumed that the gains and phases of these two devices are identical. That is, $|S_{21}|_1 = |S_{21}|_2 = B$ and $\angle S_{11}|_1 = \angle S_{21}|_2 = \psi$. If an input signal $v_i = A_o e^{j\omega t}$ is applied to the structure, the output at either drain will be $v_o = BA_o e^{j(\omega t+\psi)}$ provided that the control gate is not biased to pinchoff, in which case $v_o \approx 0$. The output of the overall structure is given by $v_o = BA_o e^{j(\omega t+\psi+\phi_n)}$, where n = the number of the control gate which is biased in the ON (positive voltage) condition. The other control gate is always assumed to be in the OFF (pinched-off) condition.

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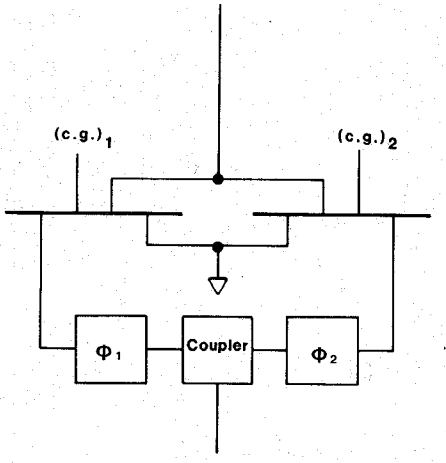

Fig. 1. Single-pole double-throw dual-gate FET switch schematic diagram.

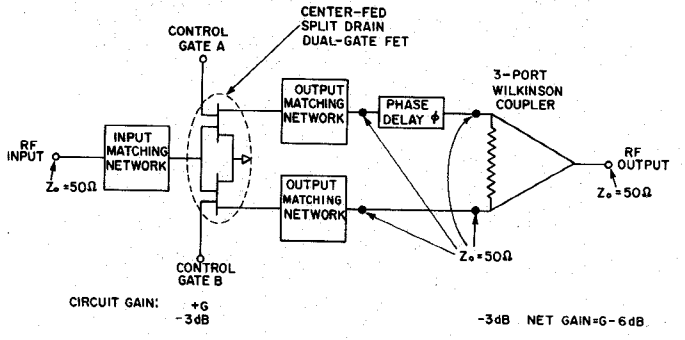

Fig. 2. Active phase-shifter circuit schematic diagram.

Thus, the phase at the output can be controlled to one of two states, making this a single-bit digital phase shifter. The amount of the phase shift is determined by the difference between ϕ_1 and ϕ_2.

The implementation of this concept into an actual active phase-shifter bit circuit is shown schematically in Fig. 2. Matching networks at the common input and the separate outputs transform the FET impedances to the 50-Ω level. The relative phase delay in one path is taken as a reference. An additional phase delay in the form of a length of 50-Ω transmission line is inserted into the other path to produce the appropriate phase shift. The circuit is completed by recombining the two output paths to a single 50-Ω terminal by means of a Wilkinson three-port coupler [9].

SPDT devices which are similar to the ones used in the phase shifter have previously been fabricated and analyzed in our laboratory [10], [11]. An equivalent circuit for the DGFET was derived from these devices for both the ON and OFF states. These were used to model the complete SPDT device. The input and output matching circuits were then designed and optimized using COMPACT (a computer-aided microwave design program) to give matched (to 50 Ω) input and output performance over a 10-percent bandwidth centered at 9.5 GHz.

The isolation between output ports of the SPDT structure has been found to be 30 dB. The DGFET itself has a dynamic range (ON-to-OFF ratio) in excess of 25 dB and a typical gain at *X*-band of between 9 and 11 dB. Since the input to the SPDT structure divides between the two channels, the signal is reduced by 3 dB. In addition, another 3 dB of power is lost into the balance resistor in the Wilkinson combiner when the circuit is operated in the normal single-channel mode. Consequently, the overall gain of the circuit is the FET gain reduced by a total of 6 dB plus any mismatch and parasitic losses developed in the microstrip circuit. This leaves approximately 3 dB of positive gain per bit in the overall circuit.

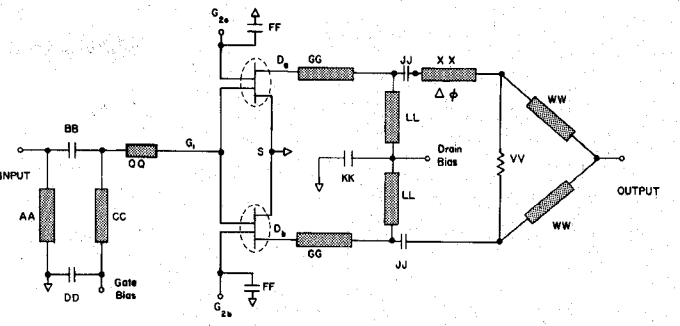

Fig. 3. Active phase-shifter circuit layout.

TABLE I
ACTIVE PHASE-SHIFTER MATCHING CIRCUIT ELEMENT VALUES

TRANSMISSION LINES				
	Electrical Characteristics		Physical Dimensions	
Element	Impedance (Ω)	Phase Length (Dg.)	Width (mm)	Length (mm)
AA	78.3	63.0	0.0220	2.006
CC	73.6	19.0	0.0270	0.603
GG	100.0	50.2	0.0086	1.616
LL	100.0	13.7	0.0086	0.440
QQ	59.0	9.0	0.0510	0.281
WW	70.7	90.0	0.0306	2.848
XX	50.0	22.5	0.0762	0.695
	50.0	90.0	0.0762	2.780
	50.0	180.0	0.0762	5.562

LUMPED ELEMENTS	
Element	Value
BB	0.31 pF
DD	15 pF
FF	7 pF
JJ	0.50 pF
KK	20 pF
VV	100 Ω

Fig. 3 shows the layout of the active phase-shifter circuit. The element values are given in Table I. Note that the circuit includes bias inputs and dc bypass circuitry for both control gates, the input gate, and both drains. The large (7, 15, and 20 pF) capacitors serve to bypass the rf signal to ground at the bias ports. The smaller capacitors are part of the matching networks and also serve as dc blocks. The drain ports are biased in parallel from the same port which leads to the topological requirement that the drain bias point be internal to (i.e., surrounded by) the rest of the phase-shifter output circuitry. We use a crossover configuration, described in Section III, to bring this signal line out to the edge of the chip where it is more easily accessible for connection to the bias supply.

As will be seen in more detail in the next section, the chip is designed to be modular. That is, for any given incremental phase shift $\Delta\phi$ between the reference arm and the phase delay arm it is necessary only to adjust the electrical length of the 50-Ω transmission line *XX*. Because the circuit is already matched to 50 Ω's at both ends of this line, its length will not effect the overall performance. Thus each phase-bit circuit is the same except for the length of that line.

III. Circuit Fabrication

The active phase-shifter circuit chips were fabricated using our standard MMIC process technology. The overriding goal in our processing is to produce a truly all-monolithic circuit in which all circuit elements (active and passive) are on-chip, and no bonding on the chip itself is required. The process technology features thin-film lumped element capacitors and resistors, air-bridge crossovers and interconnects, via-hole frontside grounding, and integral beam leads. The fabrication steps described below refer to the active phase-shifter circuit but they are essentially identical to the processes used in our other monolithic circuits and, in particular, the traveling-wave amplifier described elsewhere [12].

The material used is grown by vapor-phase epitaxy using the $AsCl_3$ system. The epitaxial structure consists of three layers. A low-doped ($<5\times10^{13}$ cm^{-3}) buffer layer is used to isolate the active device layer from the semi-insulating substrate. The buffer layer is typically 2.0 μm thick. The active, or n, layer is silicon doped at about 9.5×10^{16} cm^{-3} and is 0.4 μm thick. A thin, high-doped contact (n^+) layer is grown last to assure low specific contact resistivity for the ohmic contacts and a low source resistance. The contact layer is typically 0.2 μm thick and doped at greater than 2×10^{18} cm^{-3}.

Before acceptance for wafer processing, each slice goes through a qualification test. Wafer flatness is measured using a Tropel Interferometer, and a wafer with more than a 4-μm variation across the slice is rejected. The wafer is also subjected to a test clamping and exposure in the Zeus (model MJB-3/HP) mask aligner to assure good contact between the mask and the slice. These qualification tests are particularly important in assuring uniform prints of submicron gate and/or dual-gate patterns across the wafer.

Device isolation is achieved by a combination of mesa etching and implant isolation. To remove all of the n^+ and n layers would require a mesa step of more than 0.6 μm over which it would be difficult to achieve good step coverage particularly for the narrow gate fingers. On the other hand, using a damaging implant to compensate the n^+ epilayer with its doping levels that may go as high as 2×10^{19} cm^{-3} is not reliable. We therefore use a two-step process wherein the n^+ region around the mesa is etched away leaving a step of only ~0.2 μm. A damaging implant of $^{16}O^+$ ions—tailored to the particular doping profile—completes the isolation. This process has the added advantage of leaving surface features (the shallow mesa steps) to which subsequent layers can be aligned.

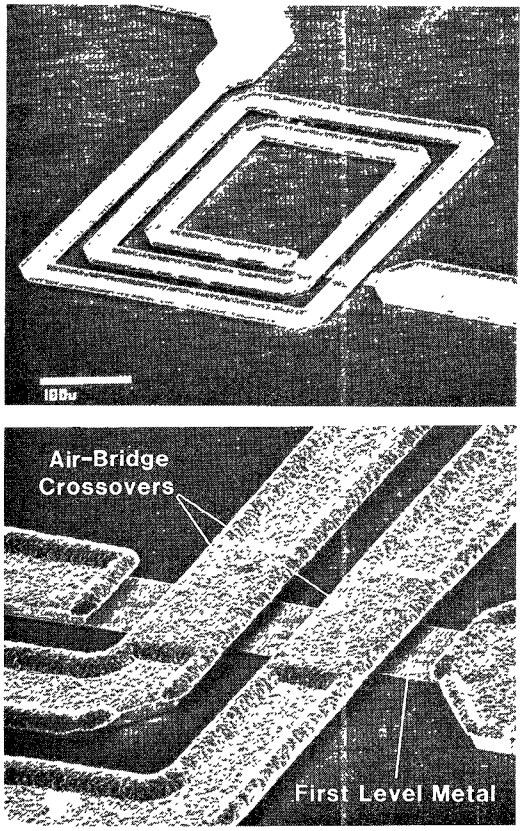

Fig. 4. Spiral inductor showing first level metal and air-bridge crossovers.

The ohmic contacts are formed of a standard Ni/AuGe metalization. We also apply a thick (5000-Å) Au layer to the sandwich which is then alloyed at 460° C for 10 s. A chloro- or bromobenzene rinse is used to enhance the source–drain metalization liftoff yield [13]. Our specific contact resistivities are typically $\lesssim10^{-6}$ Ω·cm^2. The ohmic metal is used for all shunt and series thin-film capacitor bottom plates as well as for the source and drain terminals of the FET. In addition, it is used to define the first layer metalization connection, where subsequently, a second level metal air-bridge will crossover. This is illustrated in Fig. 4, which is a SEM micrograph of a spiral inductor used in a different MMIC.

The thin-film capacitor dielectric is a plasma-assisted CVD silicon nitride layer which is deposited over the entire wafer and then patterned to leave Si_3N_4 islands covering the previously defined bottom layers. The nitride layer is oversized with respect to the bottom pad so as to completely cover it and thus minimize potential shorting problems. Where it is necessary to make contact to the bottom metal (as in a series capacitor) a finger of metal is extended out from underneath the Si_3N_4 to which a transmission line can be connected.

The nitride film is deposited in a Technics (Planar Etch II) plasma deposition system. The substrate temperature is 300° C. A plasma power of 180 W at 13.56 MHz is normally used. The plasma is struck in a mixture of 100 percent silane and anhydrous ammonia. The resultant film has a dielectric constant of about 6.8. It is nominally

5000 Å thick with a variation of about ±100 Å across the slice. A Q of around 30 has been measured at 10 GHz for these films.

The thin-film resistor material is titanium which is *e*-beam evaporated and patterned by photoresist liftoff in a conventional fashion. The resistivity of the Ti film is about 80 $\mu\Omega\cdot$cm. A glass slide with metal contacts in a known geometry is placed in the bell jar with the GaAs wafer and monitored using a four-point resistance measuring apparatus. When the appropriate thickness of Ti is deposited to give a sheet resistance of 4.4 $\Omega/\square$ (thickness $\approx$ 1900 Å) on the monitor piece, the evaporation is stopped. This technique gives thin-film resistor reproduceability of about ±5 percent.

The gate is recessed through the n^+ contact layer into the active layer. The etching is monitored by measuring the channel's saturated current until a predetermined target value is reached. The I_{ds} value used is chosen to give a pinchoff voltage of about 2 V after deposition and liftoff of the Ti/Pt/Au (1000/1000/3000 Å) gate metalization. The resist processing and exposure conditions for this masking step are rigidly controlled to assure uniform and reproducible gate prints down to ~0.7 μm. The orientation of the gates relative to the two (110) directions is critical, especially for the dual-gate structure. Because of the anisotropic nature of the gate recess etch, the gate stripes must be oriented so as to minimize undercutting of the resist stripe between the two gates.

The final processing steps on the frontside of the wafer involve the definition of the transmission-line structures, capacitor top plates, air-bridge interconnects, and integral beam leads. All of these are fabricated of plated gold about 3–4-μm thick (greater than two skin depths at X-band) and they are all defined at the same time. The technique used is a two-mask process similar to that described by other laboratories [14].

Capacitor top plates are defined undersized with respect to both the dielectric layer under them and the bottom plate metalization. Contact is then made to the top plate by means of an air-bridge interconnect. This arrangement eliminates any possibility of the capacitor shorting around the structure's edges. A SEM micrograph of a test capacitor connected to a 50-Ω transmission line by this arrangement is shown in Fig. 5. The transmission line can be seen on the right.

The air-bridges used for crossovers and interconnects are an integral part of the microstrip transmission lines that are formed on the surface of the wafer. The air gap under the plated Au is 2–3-μm high. An example of the air-bridge interconnect structure can be clearly seen in Fig. 4.

Integral beam leads are fabricated at each rf and bias port, all of which, as was pointed out earlier, are brought out to the chip edge by means of integral crossovers if necessary. The beam leads are single-ended air-bridges which extend over the chip edge, across the dicing grid region, and some distance beyond the edge of adjacent chips. As will be explained below, the chip dicing is done in such a fashion as to leave these Au ribbons intact

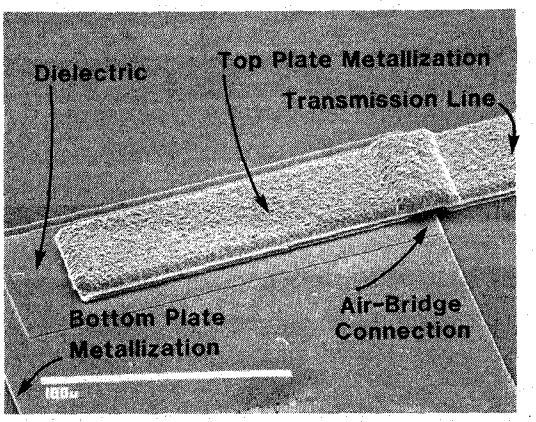

Fig. 5. Thin-film capacitor structure with air-bridge top plate connection.

extending 10–15 mils beyond the edge of the chip where they can be easily bonded to a test fixture or even directly to another chip.

After the gold plating is done, the circuit is essentially completed. The wafer is next mounted upside down for lapping on an alumina substrate. The slice is thinned from its original thickness of 15–17 mils to 100 μm. A key factor is the uniformity of this lapping. It is necessary that the back side be precisely parallel to the frontside (for the via-hole process to follow) and that the wafer be exactly 100 μm thick after lapping (to assure that the microstrip transmission lines have the correct characteristic impedances). Lapping accuracies of ±2.5 μm with uniformities across the slice also of ±2.5 μm are generally achieved.

The via holes are defined next on the backside of the wafer. An infrared aligner is used to precisely align the via-hole pattern to the target pads on the frontside of the wafer. The holes are then etched in a chemical spray or bath. The uniformity of the holes is critically related to the degree of parallelism between the two faces of the wafer. Ideally, all of the holes should "break-through" to their target pads after the same amount of etching. If not, those that come through earliest can suffer large amounts of lateral etching before the others on the wafer come through which can result in the loss of some circuits.

The final mask used determines the actual die size and shape by defining the dicing grid. This mask is aligned to the via-hole pattern now etched in the wafer. The back is selectively gold plated to a thickness of 12–15 μm in those regions between the dicing grid lines. The plated gold then acts as a mask while the GaAs is chemically etched away (using the same etch as for the via holes) in the grid lines to separate the chips. The wafer is then dismounted from the alumina substrate and the chips simply fall apart with their integral beam leads intact to be sorted and mounted.

This method of dicing has a couple of major advantages over mechanical scribing. In addition to leaving the integral beam leads intact, it is an etch and not a mechanical process so there is little stress introduced to the wafer and consequently less cracking of the final chips. Also, because wafer dicing is not dependent upon cutting or scribing along a particular crystallographic direction, chips of dif-

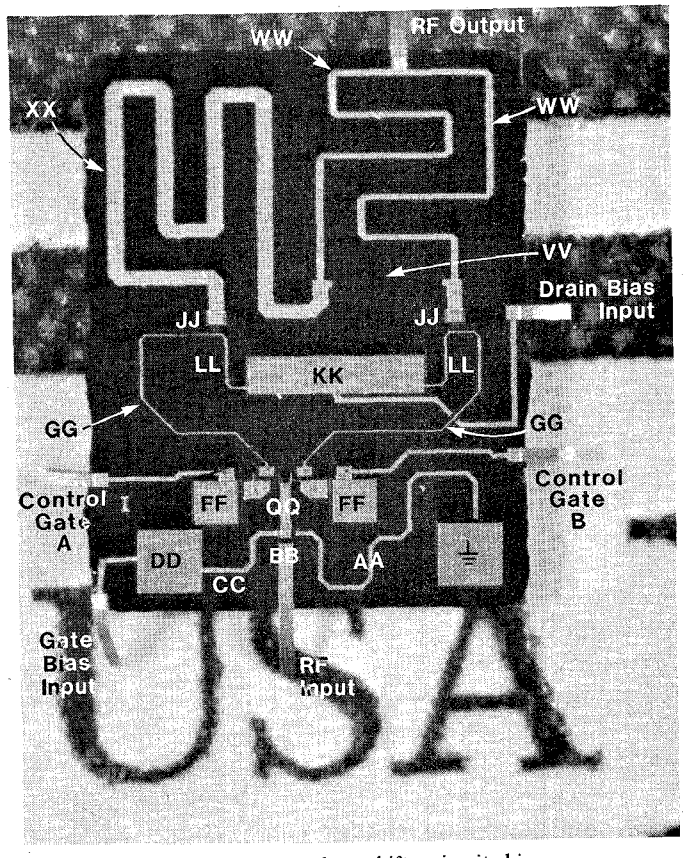

Fig. 6. Active phase-shifter circuit chip.

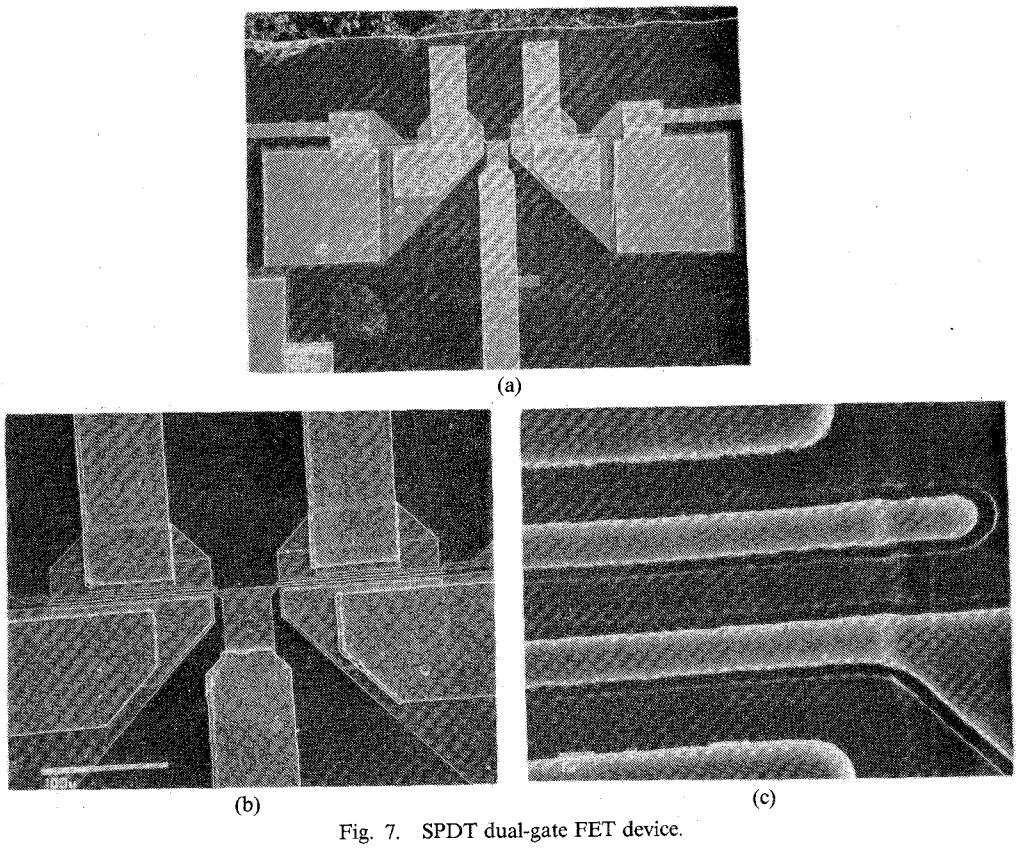

Fig. 7. SPDT dual-gate FET device.

fering sizes and shapes (even nonrectangular) can be diced from a single wafer.

Fig. 6 shows the complete active phase-shifter circuit chip (180° bit) after dicing. The various circuit elements and input and output ports are labeled as indicated in the schematic diagram in Fig. 3. Fig. 7 is a sequence of SEM

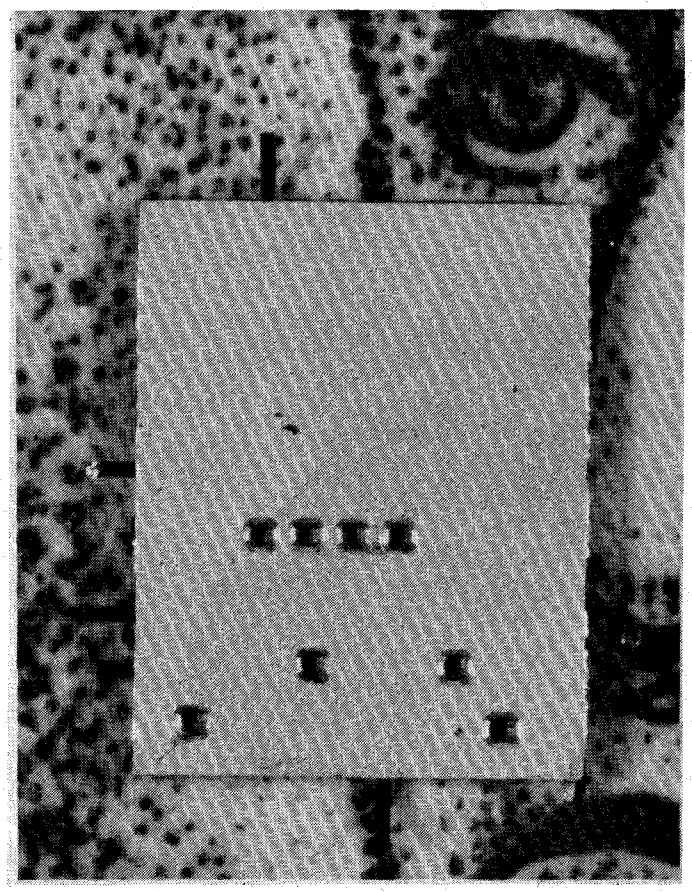

Fig. 8. Backside view of active phase-shifter circuit chip showing via holes and integral beam leads.

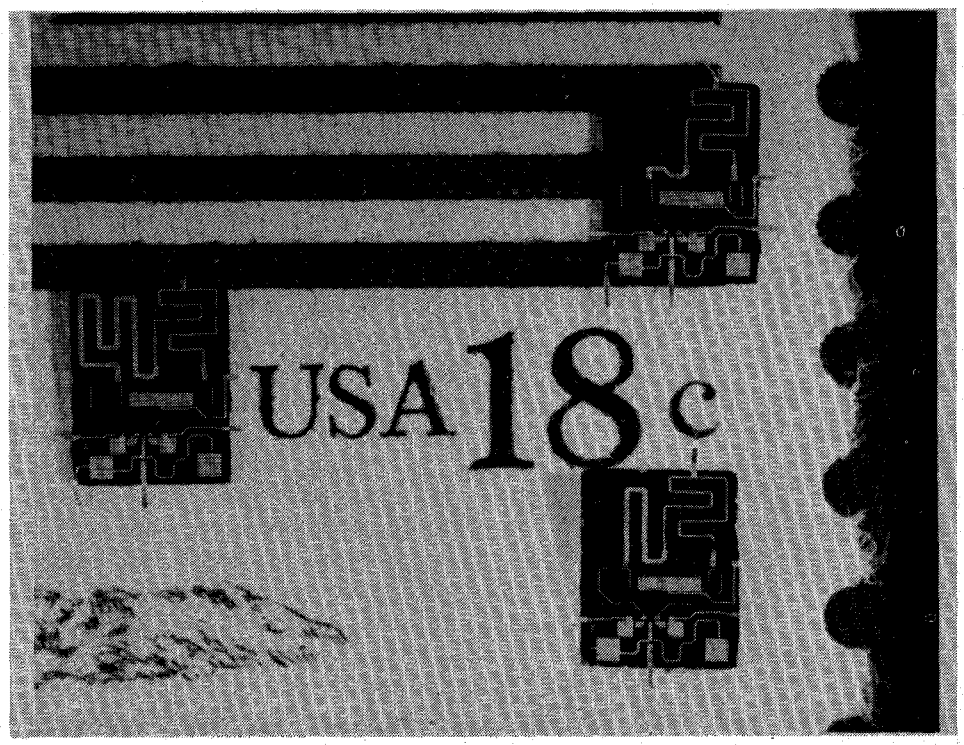

Fig. 9. Active phase-shifter circuit chips–180°, 90°, and 22.5° bits.

micrographs showing the SPDT dual-gate FET device in more detail. The feed for the T-shaped signal gate can be seen coming in from the bottom in Fig. 7(a) and (b). In Fig. 7(a) the control gate signal lines can be seen going off to either side. The square pads are the top plates of the 7-pF control gate bypass capacitors (FF). The split source

pads on the bottom of the device are both via-hole grounded. The split drains on the top define the separate 150-μm channels of the device. Fig. 7(c) is a close-up of the extreme right side of the left-hand channel showing the signal gate feed crossing the shallow mesa step and the tip of that channel's control gate. The gate lengths are nominally 1 μm with 2-μm separations between the two gates and between each gate and its adjacent ohmic contact.

As mentioned, there are via holes under both source pads which additionally serve to ground the bottom plates of the control-gate bypass capacitors. The square pads on the lower left and right of the chip (see Fig. 6) are also grounded by vias which serve to ground the signal-gate bias bypass capacitor and provide a frontside ground point for the short-circuit transmission-line stub *AA*, respectively. There is a line of four via holes under the large rectangular pad in the chip center which provide the ground for the drain bypass capacitor *KK*. Fig. 8 shows the backside of this chip in which the via holes and bottoms of the integral beam leads are clearly visible. The vias themselves are initially defined as 100-μm squares. After etching they are roughly circular at their bottom (50–100 μm in diameter) flaring out to about 200-μm square on the backside of the chip.

Fig. 9 shows three different bits of the basic phase-shifter circuit—22.5°, 90°, and 180°. Notice that the circuits are identical except for the phase-delay line in the upper left quarter of each chip. As pointed out in Section II, this modular design is possible because the outputs are matched to 50 Ω's before the phase-delay line length is inserted.

IV. Circuit Performance and Discussion

Fig. 10 presents the gain versus frequency response of a 180° bit version of the active phase-shifter circuit in both its reference state and its phase-delay state. As predicted, the gain in these two states is balanced and peaks at about 3 dB. The 1-dB bandwidth is approximately the 10-percent design value and the center-band frequency is about 300 MHz above the 9.5-GHz target. It should be emphasized that these results are for a chip simply mounted in a test fixture between 50-Ω terminals with no internal or external tuning or tweaking of any kind.

Gain balance is an important consideration in a circuit like this since the phase shifter must have the same gain response regardless of which state it is in so that only the phase shift will change with a change of state. The monolithic form of the circuit should assure good balance at least as far as the two halves of the FET are concerned since close proximity on the chip will minimize any process related variations that might be present. Good balance would not be as easy to achieve in a hybrid version of this circuit where one would have to carefully choose FET's with identical characteristics and then mount them in such a way that the parasitics introduced (e.g., bond wire lengths) were also identical. This points out a powerful advantage of monolithic technology for this kind of circuit.

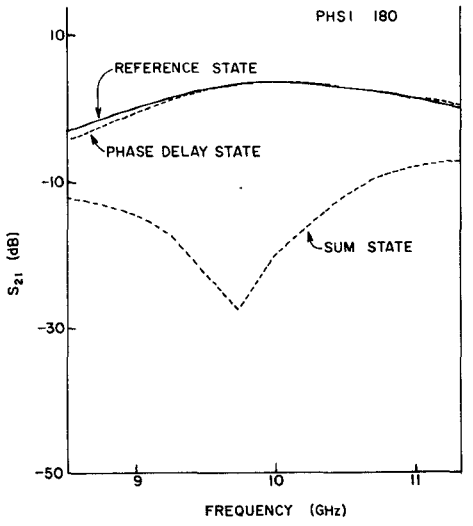

Fig. 10. 180° bit circuit gain versus frequency response.

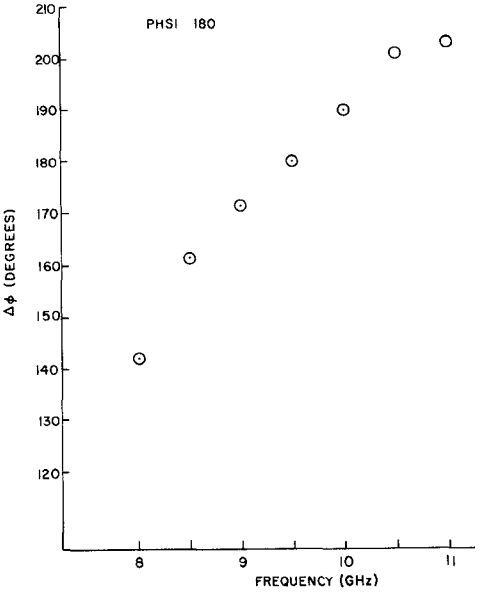

Fig. 11. 180° bit circuit phase shift versus frequency response.

The excellent balance achievable in this circuit is demonstrated not only by the matched S_{21} responses but also in the following experiment. Ordinarily, the circuit is operated with one channel ON and the other OFF. If, instead, the 180° bit circuit is operated with both channels ON and if the two paths are well balanced and exactly 180° out of phase with each other, then signals which are of equal magnitude and opposite phase will reach the Wilkinson coupler where they will be combined and should exactly cancel at the output. Such is indeed the case as seen in the sum curve presented in Fig. 10.

The phase performance of this bit is shown in Fig. 11. As expected, the phase shift between the reference state and the phase delay state is linear with frequency across the band passing through 180° right at the center-band design frequency of 9.5 GHz. This type of circuit is a true time-delay phase shifter since the phase-shifting element is

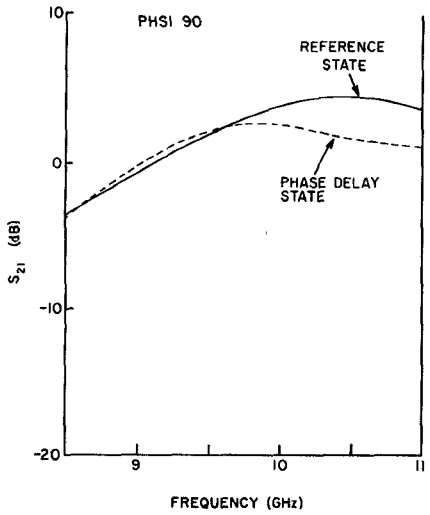

Fig. 12. 90° bit circuit gain versus frequency response.

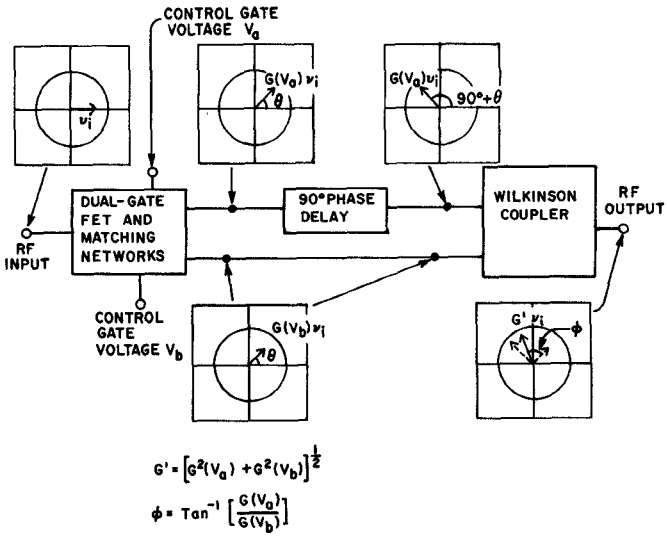

Fig. 13. Schematic diagram of vector summation of signals in 90° phase-shifter bit circuit.

a length of transmission line. As a consequence, its phase shift should have a linear frequency dependence rather than some other form such as constant. A true time-delay phase shift like this may actually be preferable in certain types of phased-array applications.

A potential difficulty with this circuit is seen most clearly in the data on one of the 90° bit circuits. Fig. 12 is the gain versus frequency response for such a circuit again showing about 3-dB peak gain and balanced performance within the design band. However, above the band a large ($\sim$3 dB) discrepancy develops in the gain response of the two states. In designing the circuit, we assumed a good match to 50 Ω at the output where the phase-delay line was connected. That being the case, the extra line length in one path should not change the overall circuit performance. However, because the output impedance of a DGFET is very high [11], maintaining a good output match across an appreciable bandwidth is a difficult design problem. Consequently, in this circuit the output match is becoming rather poor above 10 GHz. Since the phase-delay line is no longer connected to a 50-Ω impedance at these frequencies, it begins to play a role in the overall output matching network of the phase-delay state. In the 90° bit, this effect is maximized since the phase-delay line represents a quarter wavelength transformation between the output matching network and the input of the Wilkinson coupler. It may turn out to be necessary to artificially load the output of the DGFET (with a thin-film resistor, for example) to reduce the output impedance to a value which will be easier to match to over reasonable bandwidths.

Thus far, we have demonstrated how the active phase-shifter circuit can be used to achieve a discrete amount of phase shift in a digitally controlled system. This circuit and, in particular, the 90° bit version, can also be used in an analog controlled sense to achieve, simultaneously and independently, amplitude control over a dynamic range of more than 20 dB and phase control over a range of 90°. The technique used has been described by other workers [7], [8] in implementations involving hybrid circuits. It is based on the complex addition of two variable amplitude signals.

The use of the 90° bit circuit as a continuously controllable phase shifter is illustrated schematically in Fig. 13. If instead of allowing the control gates to be simply OFF or ON, they are allowed to take on a continuum of values in between, then for a given input RF voltage $v = v_i e^{j\omega t}$ the output at either port of the SPDT switchable amplifier would be a function, $G(V_{g_2})$, of the control-gate voltage V_{g_2} on that port. That is,

$$v_o = v_i G(V_{g_2}) e^{j(\omega t+\theta)}$$

where θ is the phase shift through the amplifier which, to first approximation at least, is independent of the control-gate voltage. The signal in the phase-delay channel will have an additional phase shift of $\pi/2$ with respect to the reference channel signal so that when the two vectors are summed in the Wilkinson coupler the resultant output will be

$$\begin{aligned} v' &= \frac{v_i}{\sqrt{2}} G(V_a) e^{j(\omega t+\theta+\pi/2)} + \frac{v_i}{\sqrt{2}} G(V_b) e^{j(\omega t+\theta)} \\ &= \frac{v_i}{\sqrt{2}} e^{j(\omega t+\theta)} \left[G(V_a) e^{j\pi/2} + G(V_b) \right] \\ &= \frac{v_i}{\sqrt{2}} e^{j(\omega t+\theta)} G' e^{j\phi} \end{aligned}$$

where

$$G' = \left[G^2(V_a) + G^2(V_b) \right]^{1/2}$$

and

$$\phi = \tan^{-1} \frac{G(V_a)}{G(V_b)}.$$

TABLE II

$G(V_a)$	$G(V_b)$	ϕ	G'
0	G_o	0	G_o
$0.38\ G_o$	$0.92\ G_o$	22.5°	G_o
$G_o/\sqrt{2}$	$G_o\sqrt{2}$	45°	G_o
$0.92\ G_o$	$0.38\ G_o$	67.5°	G_o

Note that the reduction of the output RF voltage v' by a factor of $\sqrt{2}$ is due to the 3-dB power splitting loss in the Wilkinson coupler.

So, by simply adjusting the control-gate voltages V_a and V_b, any phase between 0 and $\pi/2$ relative to the reference state phase θ can be realized. Furthermore, since it is the ratio of the amplitudes that determines the phase, it would be possible to keep ϕ constant while varying the amplitude of the output signal G' from an RF voltage that is $\sqrt{2}$ greater (+3 dB in power) than the maximum achievable with the reference state full ON (G_0), to a lower limit determined by the case where both channels are biased OFF (less than −20 dB).

To get complete continuous phase control over 360°, it would be necessary only to cascade a 90° bit circuit operated as a continuously variable phase bit, as described above, with one operated in the previously described digital (0° or 90°) fashion and a 180° bit circuit also operating in the digital (0° or 180°) mode. Alternatively, a four-bit digital phase shifter could be realized using this same combination of three phase-shifter bit circuits by allowing one of the 90° bits to operate in four distinct states rather than the usual two (ON and OFF). Table II shows that it is a relatively simple matter to achieve the phase states required for this digital phase shifter while simultaneously maintaining constant gain. This is accomplished by adjusting V_a and V_b to obtain particular values of $G(V)$ relative to G_o.

This mode of operation can be demonstrated in a straightforward manner by considering the case of a 90° bit active phase-shifter circuit operated with both control-gate voltages always set to the same value ($V_a = V_b = V$). Under these conditions, the gain should monotonically decrease with decreasing values of V. However, since $G(V_a) = G(V_b) = G(V)$, the phase shift through such a circuit would remain constant at 45° for all values of V. Furthermore, at some control-gate voltage less than the maximum, $G(V)$ would equal $G_o/\sqrt{2}$ and the gain of the circuit operating with the sum of equal signals will equal the reference state gain.

Fig. 14 gives the measured gain versus frequency curves of a 90° bit circuit operated as described above with various control-gate bias voltages applied. As predicted, the gain decreases as V decreases and for V in the range of 0.5 to 1 V, the combined output approximates that of the reference state. The discrepancy in the gain versus frequency response observed is due to the imbalance that exists between the reference and phase-delay states in the 90° bit as discussed previously. The phase versus frequency curves

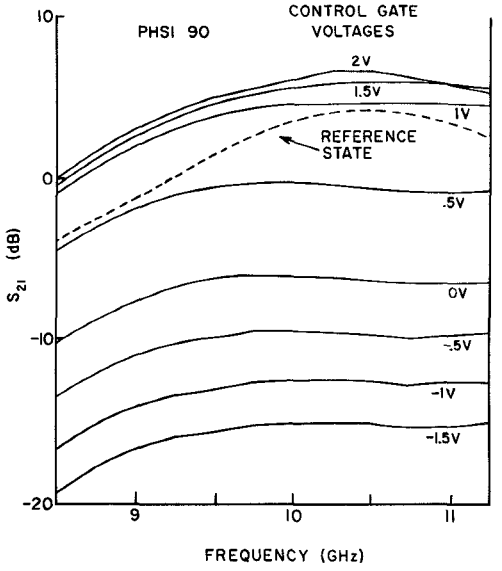

Fig. 14. Gain versus frequency as a function of control gate voltages for a 90° bit circuit operated as a 45° bit.

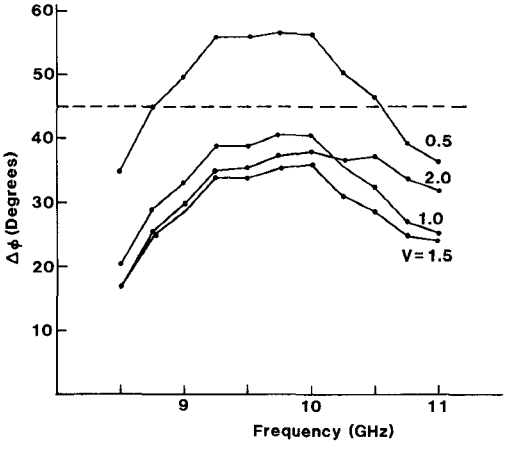

Fig. 15 Phase shift versus frequency as a function of control gate voltages for a 90° bit circuit operated as a 45° bit.

at various control gate voltages are given in Fig. 15. The data are not quite independent of control-gate voltages as predicted again because of the imbalance in the two states of the 90° bit. Nevertheless, the phase performance at all voltages is clustered near 45° relative to the reference state phase as it should be.

We have constructed a four-bit digital phase shifter out of these active phase-shifter circuits by cascading a 90° bit circuit, operated as a 45° bit in the above fashion, with a 22.5° bit, a 90° bit, and a 180° bit all operated in the normal digital fashion. The phase shifter is part of a breadboard T/R module which also includes high-power and low-noise amplification and appropriate signal switching all achieved by using various MMIC's. Details on the module will be presented in a later publication. We present here only the phase characteristics (Fig. 16) which show that the four-bit phase shifter does achieve all 16 phase states. Furthermore, the average absolute error at 9.5 GHz is less than 5° and the phase error in any one state is no

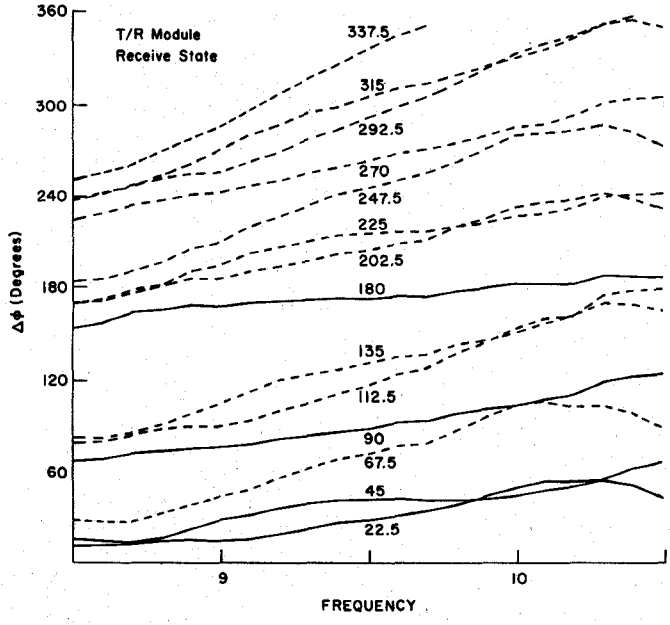

Fig. 16 Phase shift versus frequency for all states of a four-bit active phase shifter in T/R module operating in its receiver mode.

more than about half the least significant bit. We feel this is a clear demonstration of the feasibility of cascading these active phase-shifter bit circuits to achieve a practical working fully monolithic phase shifter with gain suitable for phased-array applications.

V. Conclusions

In this paper, the design, fabrication, and characterization of a monolithic FET digital phase-shifter circuit was described. The circuit is based on a SPDT dual-gate FET switchable amplifier design. The all-monolithic circuit included all rf matching and bias circuitry on a 2.5×3.0×0.1-mm chip. The fabrication technology used to make these MMIC's was described in some detail. The technology features the following key elements: Thin-film Si_3N_4 MIM capacitors for RF tuning, blocking and bypassing applications; thin-film Ti resistors; air-bridge RF/dc cross-overs and interconnects for contacting capacitor top plates; via holes for selective frontside circuit grounds; and, integral gold beam leads to eliminate any on-chip bonding.

The circuit demonstrated about 3-dB gain across a 10-percent band centered near 9.5 GHz. Excellent balance was demonstrated within this band between the reference and phase-delay states. True time-delay phase shifting was also demonstrated. A technique was described for using the 90° bit circuit as a continuously variable phase shifter with amplitude control. Operation of this circuit in this mode was verified by demonstrating 45° phase-shifting operation over a range of output amplitudes. Finally, a cascade of four phase-shifter circuit chips was used to demonstrate all 16 phase states of a 4-bit digital 360° phase shifter in a T/R module application.

Monolithic GaAs microwave integrated circuits hold great promise for helping to realize the goal of practical phased-array antenna systems. The phase shifter is a key element in any such system and the active phase-shifter circuit described in this paper has shown the kind of performance in an all-monolithic form which will help make the goal of electronically agile arrays a reality.

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References

[1] M. E. Davis, "Integrated diode phase-shifter elements for an *X*-band phased-array antenna," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-23, pp. 1080–1084, Dec. 1975.

[2] A. Rosen, R. U. Martinelli, A. Schwarzmann, G. J. Brucker, and G. A. Swartz, "High-power, low-loss p-i-n diodes for phased-array radar," *RCA Rev.*, vol. 40, no. 1, pp. 22–58, Mar. 1979.

[3] C. Tsironis and P. Harrop, "Dual-gate MESFET phase shifter with gain at 12 GHz," *Electron. Lett.*, vol. 16, pp. 553–554, July 1980.

[4] C. Tsironis, P. Harrop, and M. Bostelmann, "Active phase shifters at *X*-band using GaAs MESFETs," in *IEEE Int. Solid-State Circuits Conf. Dig.*, New York, 1981, pp. 140–141.

[5] R. S. Pengelly, C. W. Suckling, and J. A. Turner, "Performance of dual-gate GaAs MESFET's as phase shifters," in *IEEE Int. Solid-State Circuits Conf. Dig.*, New York, 1981, pp. 142–143.

[6] M. Kumar, R. J. Menna, and H. Huang, "Broad-band dual-gate FET continuously variable phase shifter," in *IEEE MTT-S Intl. Microwave Symp. Dig.*, Los Angeles, 1981, pp. 431–433.

[7] M. Kumar, R. J. Menna, and H. Huang, "Broadband active phase shifter using dual-gate MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 1098–1102, Oct. 1981.

[8] Y. Gazit and H. C. Johnson, "A continuously variable *Ku*-band phase/amplitude control module," in *IEEE MTT-S Intl. Microwave Symp. Dig.*, Los Angeles, 1981, pp. 436–438.

[9] R. C. Waterman, Jr., W. Fabian, R. A. Pucel, Y. Tajima, and J. L. Vorhaus, "GaAs monolithic Lange and Wilkinson couplers," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 212–216, Feb. 1981.

[10] W. Fabian, J. L. Vorhaus, J. E. Curtis, Sr., and P. Ng, "Dual-gate GaAs FET switches," presented at the IEEE GaAs Integrated Circuit Symp. (Lake Tahoe, Nevada), Sept. 1979.

[11] J. L. Vorhaus, W. Fabian, P. B. Ng, and Y. Tajima, "Dual-gate GaAs FET switches," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 204–211, Feb. 1981.

[12] Y. Ayasli, R. Mozzi, J. L. Vorhaus, L. Reynolds, and R. A. Pucel, "A monolithic GaAs 1 to 13 GHz traveling-wave amplifier," this issue, pp. 976–981.

[13] M. Hatzakis, B. J. Canavello, and J. M. Shaw, "Single-step optical lift-off process," *IBM J. Res. Develop.*, vol. 24, pp. 452–460, July 1980.

[14] T. Suzuki, M. Kobiki, M. Wataze, K. Segawa, and M. Irie, "Plated source bridge (PSB) GaAs power FET with improved reliability," in *IEEE MTT-S Intl. Microwave Symp. Dig.*, (Los Angeles), 1981, pp. 34–36.

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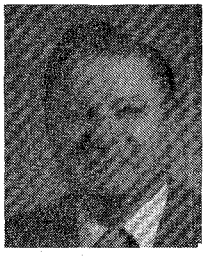

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New Technology Towards GaAs LSI/VLSI for Computer Applications

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Abstract—**For future large-scale computer applications, new device technologies towards GaAs LSI/VLSI have been developed: self-aligned fully implanted planar GaAs MESFET technology and high electron mobility transistor (HEMT) technology by molecular beam epitaxy (MBE). The self-aligned GaAs MESFET logic with 1.5-μm gate length exhibits a minimum switching time of 50 ps and the lowest power-delay product of 14.5 fJ at room temperature. The enhancement/depletion (E/D) type direct coupled HEMT logic has achieved a switching time of 17.1 ps with 1.7-μm gate length at liquid nitrogen temperature and more recently a switching time of 12.8 ps with 1.1-μm gate HEMT logic, which exceeds the top speed of Josephson Junction logic and shows the highest speed of any device logic ever reported. Optimized system performances are also projected to system delay of 200 ps at 10-kilogate integration with GaAs MESFET VLSI, and 100 ps at 100-kilogate with HEMT VLSI. These values of system delay correspond to the computer performance of over 100 million instructions per second (MIPS).**

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I. INTRODUCTION

FUJITSU'S latest large-scale general purpose computer, using Si-based technology, has already achieved speeds as high as 30 Million Instructions Per Second (MIPS). In

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